



Seventeenth Annual Single Event Effects Symposium

Preliminary Technical Program

Monday, April 14

5:00 – 8:00 PM	Registration/ Reception	<i>Sienna Room/ Renaissance Foyer</i>
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Tuesday, April 15

7:00 – 8:30 AM	Continental Breakfast	<i>The Foyer, Long Beach Renaissance</i>
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8:30 AM C. Poivey

Welcome and Local Arrangements

8:35 AM J. Black

Introduction to Technical Program

INVITED TALK

8:40 AM R. Weller

Session A: Devices and ICs: Memory

9:05 AM A. Tipton, M. Xapsos, H. Kim, M. Friendlich, M. Campola, C. Seidleck, K. LaBel, J. Hutson, J. Pellish, R. Baumann, X. Deng, A. Marshall, G. Boselli, M. Mendenhall, R. Reed, R. Schrimpf, R. Weller

Heavy Ion and Proton Irradiations of 65 nm SRAMs

9:30 AM X. Yao, D. Patterson, L. Clark

Heavy Ion Induced Single Event Upsets in Unhardened SRAM

9:50 AM S. Doyle, N. Haddad

SEU Immune 16M SRAM Development and Validation

10:10 AM E. Kanyogoro, M. Peckerar, H. Hughes, P. McMarr, M. Liu

New Materials for Mitigating Linear Energy Transfer Sensitivities in Highly Scaled Submicron CMOS Technology SRAM Cells

10:30 AM **Break**

10:00 AM –
10:00 PM **Industrial
Exhibits Open**

10:50 AM	P. Marshall, K. Label, M. Friendlich, C. Seidleck, M. Berg, A. Phan, J. Schwank, M. Shaneyfelt, P. Dodd, K. Rodbell, D. Heidel, M. Xapsos, A. KleinOsowski, M. Hakey	Proton, alpha Particle, and Heavy Ion SEU Test Results in 65 nm SRAMs Fabricated in IBM's SOI Process
11:10 AM	N. Gupta, B. Vermeire, H. Barnaby, M. Goksel, E. Li, D. Czajkowski	Design of a 4 Gb Radiation Hardened NAND Flash Memory
11:30 AM	T. Oldham, M. Suhail, M. Friendlich, M. Carts, N. Helmond, H. Kim, M. Berg, C. Poivey, S. Buchner, A. Sanders, K. Label	SEE Response of Advanced 4G NAND Flash Memories
11:50 AM	G. Allen, C. Carmichael, G. Swift	Status of the XRTC Static, Dynamic, and Upset Mitigation Test Campaign on the Virtex-4 Family of Aerospace-Grade Reconfigurable FPGAs

12:10 PM **Lunch**

Session B: Devices and ICs: Mixed-Signal

1:30 PM	C. Hafer, M. Lahey, D. Harris	Single Event Effects Results for a RadHard Medium Scale Integration Circuit Family
1:50 PM	M. Carts	Philips SA8016DH, 2.5 GHz Synthesizer SEE Testing
2:10 PM	C. Kuznia, J. Ahadian, R. Pommer, R. Hagan	SEU Testing of a Multi-Gbps Fiber Optic Transceiver Operating Over Parallel Ribbon Fiber
2:30 PM	B. Olson, W. Holman, L. Massengill, P. Fleming	Single-Event Effect Mitigation in Switched-Capacitor Comparator Designs
2:50 PM	K. Kruckmeyer, B. Brown, J. Prater, S. DasGupta	Unexpected SET Dependence on Operating Conditions for a Digital to Analog Converter

3:10 PM **Break**

3:30 PM	S. Whitaker, L. Miles, L. Davis, J. Gambles, G. Maki, B. Gilbert, B. Randall, N. Harff	Multiple Upset Radiation Tolerant Combinational Logic Structure
3:50 PM	D. Loveless, L. Massengill, B. Bhuvu, W. Holman	A Radiation-Hardened-by-Design Voltage-Controlled-Oscillator for Mixed-Signal Phase-Locked Loops

Session C: SET Mechanisms and Modeling

4:10 PM	N. Renaud, C. Heng, D. Truyen	Single Event Transient Characterisation of a CMOS 180nm Technology by 3D Simulation and Radiation Testing
4:30 PM	D. McMorro, V. Ferlet-Cavrois, P. Paillet, J. Baggio	Single-Event Transient Propagation in Combinational Logic
4:50 PM	V. Pouget, A. Douin, D. Lewis, P. Fouillat	Characterization of Single Event Transient Broadening in 130nm Inverters Chains

5:30 – 10:00 PM **Reception/
Industrial Exhibit**



Seventeenth Annual Single Event Effects Symposium

Wednesday, April 16

7:00 – 8:30 AM	Continental Breakfast	<i>The Foyer, Long Beach Renaissance</i>
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INVITED TALK

8:30 AM S. Moss

Session D: Devices and ICs: Reconfigurable

9:00 AM	S. Rezgui, J. Wang, Y. sun, J. McCollum, B. Cronquist	SET Propagation in Flash-Based FPGAs
9:20 AM	C. Carmichael, G. Swift, G. Allen	Test Techniques and Lessons Learned: The XRTC Virtex-4 SEE Test Campaign
9:40 AM	H. Quinn, P. Graham, B. Pratt	An Automated Approach to Estimating Hardness Assurance Issues in Triple-Modular Redundancy Circuits in Xilinx FPGAs
10:00 AM	G. Miller, G. Swift, C. Carmichael	Upset Test Methodology and Results for a Mitigated-by-TMR MicroBlaze Soft-Core Processor

10:20 AM	Break	
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10:50 AM	K. Morgan, M. Caffrey, M. Dunham, P. Graham, H. Quinn, C. Carmichael, T. Duong, A. Lesea, G. Miller, G. Swift, C. Tseng, Y. Wu, R. Monreal, G. Allen	Upset-Induced Failure Signatures, Recovery Methods, and Mitigation Techniques in a High-Speed Serial Data Link for Space Applications
11:10 AM	C. Tseng, C. Carmichael, G. Swift, G. Allen	Optimized Virtex-4 FPGA Self Hosting Configuration Management
11:30 AM	M. Berg, C. Perez, H. Kim	Investigating Mitigated and Non-Mitigated Multiple Clock Domain Circuitry in a Xilinx Virtex-4 Field Programmable Gate Array

11:50 AM	Lunch	
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Session E: SEE Mechanisms and Modeling

1:10 PM	N. Haddad	More in Support of Secondary Particle Upset in SEU Hardened-by-Design Memory
1:30 PM	R. Ladbury	Bounding SEE Rates: Model Selection and Data Requirements

1:50 PM	K. Lilja, A. Azarenok, M. Baze, B. Hughlock	Comparisons of simulated and measured SEUs for large angle of incidence in 90nm technologies
2:10 PM	M. Liu, H. Hughes	Estimating Limiting Upset Cross Section of 6T SOI SRAMs
2:30 PM	S. DasGupta, T. Roy, O. Amusan, M. Alles, A. Witulski, L. Massengill, B. Bhuva, R. Schrimpf, R. Reed,	Lessons from TCAD Modeling of Advanced Processes

2:50 PM	Break	
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3:10 PM	Panel Discussion	Uncertainty in Predicting Single Event Effect Rates Chair: Ray Ladbury
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6:00 – 8:00 PM	Happy Hour	
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Seventeenth Annual Single Event Effects Symposium

Thursday, April 17

7:00 – 8:30 AM	Continental Breakfast	<i>The Foyer, Long Beach Renaissance</i>
<u>INVITED TALK</u>		
8:30 AM	J. Schwank	
Session F: Testing Issues		
9:00 AM	M. Baze, J. Tostenrude, D. Hogue, J. Clement, J. Braatz, F. Nelson, J. Wert	SEE Test Strategies and Results for SoC Analog Function Blocks
9:20 AM	J. Ahlbin, J. Black, L. Massengill, O. Amusan, A. Balasubramanian, M. Casey, D. Black, M. McCurdy, R. Reed, B. Bhuva	C-CREST Technique for Combinational Logic SET Testing
9:40 AM	C. Poivey, D. Peyre, C. Binois, F. Sturesson, F. Bezerra	Test Protocols for Single Event Burnout (SEB) and Single Event Gate Rupture (SEGR) Characterization of Power MOSFET Transistors
10:00 AM	S. Liu, M. Zafrani, H. Cao, R. Berberian, C. DiCizzeno, M. Boden	Vulnerable Trench Power MOSFETs Under Heavy Ion Irradiation
10:20 AM	Break	
10:40 AM	K. Label, L. Cohn	Radiation Testing, Characterization and Qualification Challenges for Modern Microelectronics
11:10 AM	A. Balasubramanian, B. Bhuva, L. Massengill, B. Narasimhan, W. Holman	A Built-In Self-Test (BIST) Technique for Hardness Assurance against SETs in Digital Circuits
11:20 AM	I. Troxel, P. Murray, R. Monreal, P. Rutt	SEE Characterization Methods for Internet Protocol Routing and Ethernet Networking Devices in Space
11:40 AM	K. Warren, A. Sternberg, B. Sierawski, R. Reed, R. Weller, C. Carmichael, G. Swift, J. De Jong, J. Fabula, L. Massengill	A Step Closer to Virtual Irradiation: Coupling Circuit Level Simulation and Radiation Transport Tools for Evaluating the Single Event Upset Response of a Radiation Hardened Latch
12:00 PM	E. Petersen	Problems and Opportunities in Fitting SEU Heavy Ion Data and Cross Section Curves
2:30 PM	Volleyball Session	